Amendments in the Specification:

The specification has been amended to provide consistency with the amended drawings and to correct minor errors. No new matter has been added. Replacement paragraphs are provided below.

Please replace the paragraph beginning on page 4, line 9, and ending on page 4, line 28, of the original application as filed with the following:

With reference to Fig. 1, a first memory cell 15 of a non-volatile transistor memory array has first and second programming lines 11 and 13, associated with respective contacts 22 and 26, as well as bit lines 17 and 37 and word line 19 all running through the cell and into neighboring cells. In particular, programming lines 11 and 13, bit line 17 and word line 19 run into neighboring cell 115 in a first direction, while bit line 37 runs into neighboring cell 215 in a second direction. Word line 19 is in a capacitive relation to a polysilicon plate, forming capacitive device ~~gates of transistors~~ 25 ~~and 125~~. Word line 119 similarly relates to another polysilicon plate (130, shown in Fig. 2) forming capacitive device 125. Each memory cell has an EEPROM memory transistor 23 and a current injector including a fast diode 29, with a cathode [[28]] connected to an electrical contact 22 and to an electrode of an MOS injector transistor 21. The injector transistor 21 has a single poly control gate (represented by 21A, 21B), described below. MOS injector transistor 21 is biased by either actuation line 36 (21A), or by means of capacitive coupling via word line 19 (21B), or both, depending on the mode of operation. The anode of diode 29 is connected to the transistor substrate and electrical contact 24. Biasing of first program line 11 of transistor 21 provides reverse bias to diode 29. Such reverse bias generates current toward the depth of the substrate.

Please replace the amended paragraph beginning on page 4 and ending on page 5 of the filed Amendment dated 12/5/2005 with the following:

In the memory cell 15 of Fig. 2, two programming lines 11 and 13 control operation of injector transistor 21 that can reverse bias diode 29. Recalling that this reverse bias of diode 29 generates impact ionization current that stores charge in the floating gate of memory transistor 23. But memory transistor 23 was said to have a device 25 in a capacitive relation with respect to word line 19. The device 25 has a polysilicon plate 30 having a first finger or tang 86' that serves as control gate of memory transistor 23 actuated by word line 19. The word line 19 may be over or under plate [[25]] 30, separated by an insulative layer, such as oxide. In the case of being under plate [[25]] 30, the word line 19 may be a buried word line in an n-well diffusion in order to save space. Another tang 186 extends out of memory cell 15 to an adjacent injector transistor as a control gate for the injector. Voltage on the word line 19 is capacitively coupled to plate 30 thereby providing voltage for erasing EEPROM memory transistor 23. Simultaneously, the plate provides a voltage to a control gate of an injector transistor in an adjacent cell. In other words, each injector transistor has a control gate that is a tang of a polysilicon plate, such as plate 30. In the case of injector transistor 21, tang 76' projecting from polysilicon plate 130 provides voltage via capacitive coupling with word line 119. Recall that voltage bias on line 33 charges line 36, stimulating impact ionization from diode 29 that passes through a common substrate toward memory transistor 23. Since line 36 serves as floating gate for the memory transistor, the floating gate remains charged, even after bias is removed from line 31. The role of tang 76' is to augment voltage applied to the control gate of transistor 21 and to allow word line control of

programming. In the latter mode of operation, an entire row (or column) of memory cells could be programmed or erased under word line control. In the former mode of operation, some of the voltage for programming or erasing is coupled through a word line, but another part of the needed voltage is supplied by a voltage applied on line 33, thereby allowing programming and erase control of individual cells. The circuit topology of Fig. 2 is closer to an actual layout of a cell, compared to Fig. 1, because word lines are at right angles to bit lines.

Please replace the paragraph beginning on page 9, line 4, of the original application as filed with the following:

In Fig. 3, the via 97 communicates with current meter 39, seen in Figs. 1 and 2, through contact 32. Memory transistor 23 has a control poly gate 86 spaced between drain ~~source~~ 82 and source ~~drain~~ 84, in turn communicating through vias 97 and 99 to the drain ~~source~~ 82 and the source ~~drain~~ 84. Subsurface region 93 connected by via 94 for external contact is actuation line 133 for bias of the second memory cell 115 in Fig. 1. Recall that transistor 23 has a floating gate formed three gate leads for transistors 35, 21, and 22 seen in Figs. 1 and 2. The gate leads are represented by dashed line 85 in Fig. 3. Control gate 86 is a tang 86N of poly plate 30 of device [[23]] 25 seen in Fig. 2. Contact 32 is associated with current meter 39 on line 37. Each well may have a current meter although only the current meter 39 associated with measuring charge on a memory cell is discussed herein.

Please replace the amended paragraph beginning on page 6, 2nd paragraph, and ending on page 7 of the filed Amendment dated 12/5/2005 with the following:

In Fig. 3, the transistor 223 is a memory transistor of an adjacent cell. The transistor 223 is symmetric with transistor 23 having a shared electrode 84 and ~~source~~ drain electrode 88. Via 101 connects drain electrode 88 to a drain contact. The via 99 above shared electrode 84 forms a plane of symmetry except for current measuring electrodes and provides bias for associated transistors 23 and 223, similar to via 90 and subsurface region 91, but using actuation line [[201]] 103 seen in Fig. 4. Control poly region 92 is a tang of another poly plate and so is poly region 176 of injection transistor 221. The floating gate for memory transistor 223 is actually formed by three gate leads, analogous to the leads of transistors 35, 21, and 23, indicated by dashed line 185. To the right of p-well 65 is p-well 67, separated by isolation region 77. The doped n-implants 162 and 164 are in p-well 67, below conductive vias 172 and 174. The implants 162 and 164 define electrodes for MOS injection transistor 221. A cooperating part of the current injector is formed by a diode having p-implanted region 181 abutting n+ region 162. The diode is made by implants at the same time and in the same manner as the diode associated with transistor 21. The diode is controlled by transistor 221, having control gate 176, operating in the same manner as transistor 21. Electrons for charge storage on floating gates 85 and 185 are generated by this impact ionization. These electrons are involved in transfer to the floating gates by tunneling hot electron injection or other known mechanisms.

Please replace the amended paragraph beginning on page 7 of the filed Amendment dated 12/5/2005 with the following:

One of the remarkable features of the present invention is illustrated in Fig. 4. The word line 19 is seen to lie under or over poly plate 30. The poly plate 30 has a pair of tangs 86' and 186, extending in opposite directions. The tang 86' is the control gate 86 of memory transistor 23. See Fig. 3. The tang 186 is the control gate of an injector transistor in another row. Voltage on word line 19 induces voltage on poly plate 30, a capacitor-like device. Tang 86' causes erasing of memory cell 23 while tang 186 initiates impact ionization current in an injector transistor in another row and hence writing in another row. This is similar to action by poly plate 130, spaced over or under word line 119 by an insulative layer, such as oxide, and having tang 76 projecting into injector transistor 21 as its control gate. Voltage on word line 119 induces voltage on poly plate 130 and hence on tang 76. This voltage initiates impact ionization current that stores charge in the floating gate of memory transistor 23. ~~Shared line 101~~ Via 99, a common electrode for memory transistor 23 and 223 in Fig. 3, is an axis of symmetry for structures to the right, except for current measuring lines. Lateral symmetry allows two memory transistors to share the same well and achieve a good degree of compactness.

Please replace the paragraph beginning on page 12, line 5, and ending on page 12, line 19, of the original application as filed with the following:

In Fig. 8, word line 19 is shown an example of diffused p+ layer in n-well [[119]] 140 between isolation regions 132 and 134. The n-well 119 is formed in the p-type substrate 136. By diffusing the word line in the substrate, the word line geometry is made more compact. A layer of oxide 138 is deposited to a thickness of at least 1500 Å before the poly plate 43 is deposited. Poly plate 43 has the usual thickness of a control gate, perhaps 3000 Å. The diffused word line 19 runs under a plurality of poly plates, for example, all of the poly plates in a row. Whether the poly plates are diffused under the word line or not, all of the poly plates associated with one type of control gate in a row of memory cells are aligned under or over the word line in parallel relation therewith.